USC Viterbi School of Engineering

EE 457 Computer Systems Organization
Units: 4
Spring 2019 – Tues. Thurs. 12:00-1:50PM in OHE230
Tues. Thurs. 5:00-6:50PM in OHE136

Instructor: Gandhi Puvvada
Office: EEB 238
Office Hours: 4:10-6:00PM Mon and 2:30-4:30 PM Wed
either in EEB 238 or in EEB203
Gandhi_Office_Hours_Sp2019.pdf
Contact Info: gandhi@usc.edu,
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Teaching Assistants:
EE457 TA -- Tanvir Manhotra <manhotra@usc.edu>
EE457 TA -- Shreya Shivayogi Turmari <turmari@usc.edu>

Mentor: Spandan Kanubhai Kachhadiya <kachhadi@usc.edu>

Office: PHE330 **Office Hours of TAs and Mentors**
https://www.dropbox.com/s/xjt4g089qxu5zfq/EE457_Office_Hours_Spring2019.pdf?dl=0

1. Course Description

This course covers computer organization and design. It provides CS/CE/EE students with a substantial understanding of a CPU at its logic design level. Design of the control unit and the data path unit of a simple multi-clock-cycle CPU and a pipelined CPU is covered in detail. Computer arithmetic and memory hierarchies (cache, main memory, virtual memory) are also covered. Hardware support for exceptions, dynamic scheduling of instructions (Tomasulo algorithm to execute instructions in an out-of-order fashion), branch prediction, multi-threaded cores, multi-core processors with cache coherency, locks and mutual exclusion among threads via special atomic instructions are also discussed in detail. Students design in Verilog and use ModelSim simulator to verify their RTL design/simulation exercises.

2. Learning Objectives

At the end of the course, students are expected to feel confident to perform logic design of a CPU or any hardware system utilizing pipelining and other RTL techniques and proceed to graduate courses in computer architecture or general hardware design. This course is also expected to improve students' design skills and analytical skills.

3. Course administration

a) Course prerequisites: EE354L (previously EE254L or EE201L) Introduction to Digital Circuits is a *necessary* prerequisite. Undergraduate students without this prerequisite will not be able to do this course. Graduate students are expected to have taken a logic design course and a course covering some assembly language in their undergraduate course work before taking this course.

Recommended Preparation: Familiarity with the following items at an introductory level is expected.

1. Programming in an assembly language of any processor (CISC or RISC)
2. Digital Logic design at RTL level (Register Transfer Language Level)
3. Design entry using Verilog HDL (Hardware Description Language) and simulation

b) Classes: http://classes.usc.edu/term-20181/classes/ee-457

Discussion class is *not optional*. Homeworks and lab assignments are primarily discussed during the discussion class. Important additional material may be covered in the discussion class.

c) Examinations: No makeup exams.

Please note that EE457 exams are long (3 Hours) as they are design exams.

One quiz (~10%), one midterm (~24%), and the final exam (~33%)

The "Quiz" slot (Qz **TBA** ➔ Thursdays 5-8:00PM))
We will utilize the quiz slot only twice in the whole semester to conduct a quiz and a midterm exam. So, it is OK to have schedule conflict with the quiz slot provided you agree to make yourself available for these two occasions.

Quiz (about 10%): Thursday Feb. 7, 2019 05:00 PM - 08:00 PM PST
Midterm (about 24%): Thursday Mar. 21, 2019 05:00 PM - 08:00 PM PST

April 5 (Friday)	Last day to drop a class with a mark of "W"

https://classes.usc.edu/term-20191/calendar/

Note: EE457 Final Exam is listed under the Exceptions Schedule posted at the bottom of:
https://classes.usc.edu/term-20191/finals/
Final Exam (about 33%): Tuesday, May 7, 2019 either 3:30 PM to 6:30 PM or 4:30 PM - 7:30 PM PST
Official slot is 4:30 PM to 6:30 PM. With your cooperation, I am extending it by 1 hour by either starting the exam 1 hour early or ending the exam 1 hour late. We will check with all the students to see if one of the two choices works for everyone. We may end up conducting the final exam at two times as stated above if we do not have a single choice acceptable to all. I am hoping that at least one of the two choices fits every student. Please let me know if both choices do not work for you.

d) Grading Policy:

Course weights	Percentage	
Assignments		Late submission penalty for assignments
Homeworks	about 7%	5% penalty per day up to 3 days if solution is not given out
Labs	about 26%	3% flat penalty up to 3 days
Exams		
Quiz	about 10%	**no make-up exam**
Midterm	about 24%	**no make-up exam**
Final	about 33%	**no make-up exam**
Penalty for lecture absence: 1% of the course for the 4th and the 5th; 2% for the 6th and there after		
Penalty for discussion absence: 0.5% for the 4th and the 5th; 1% for the 6th and there after		

e) Academic Accommodations:

Any student, requiring academic accommodations based on a disability, is required to register with the Center for Academic Support and Disability Services and Programs (CAS & DSP) each semester.

An online profile can be created on **MyDSP** .
A letter of verification for approved accommodations can be obtained from CAS & DSP.
Please make sure that the letter is delivered to me as early in the semester as possible
(no less than 2 weeks before an exam).
The CAS & DSP office is located in GFS 120.
Their phone number is (213) 740-0776. Email: **ability@usc.edu**
http://dsp.usc.edu/accommodations/

f) Miscellaneous administrative matters:

Lecture class attendance, penalty for absence, and minimum required performance:

If you miss more than 2 lecture meetings, you will start noticing that you are falling behind.
If you miss more than 5 lecture meetings, you may as well drop the course.
It is a design course requiring continuity in your learning process. So please attend every lecture meeting.
The following penalty rules do not apply to remote students, as I cannot monitor their attendance. They are allowed to watch the lecture in the evening/late night. But they should finish watching lectures of a week wihin that week and send an email to the instructor stating that they watched the week's lectures.
Penalty for lecture absence: 1% for 4th, 5th; 2% for 6th and after.
Penalty for discussion absence: 0.5% for 4th, 5th; 1% for 6th and after.
http://www-classes.usc.edu/engr/ee-s/457/EE457_attendance_policy.html

Homeworks shall be done individually. *In-class exercises (but not short exercises posted on D2L) can be done taking help from fellow students but each student shall submit individually his/her completed work.*
Design and simulation labs can be performed either individually or in teams of two students (2 per team).
But occasionally, design labs may be assigned as individual assignments.
Teams shall submit only one set of Verilog code and results online.
However, justifications/explanations, state diagrams, and answers to questions at the end of the lab assignment (**paper submissions), shall be prepared individually.**
Copying is different from discussing ideas with other students.
You are encouraged to share your thoughts on homework, design labs, and design lab reports with other students as long as one of you act as a *Teaching Assistant* who tries to help without giving away the solution.

Absolutely no copying. Do NOT try to copy any assignment. We have ways to find if a design/simulation lab has been copied.
Try not submitting a non-working lab as we give very little credit for a non-working lab.
We are here to help you and guide you in your debugging. If you submit a **non-working design/lab** and if do not write on the top of it in **BIG** letters that it is NOT WORKING (and further do not inform the instructor, the TAs, and the lab graders through an email before submission), we will treat it as an attempt to cheat. This is very important.

Academic dishonesty cases will be dealt with severely. Please go through the short tutorial on Academic Integrity at USC posted at
https://libraries.usc.edu/research/reference-tutorials
Try to see which version works for you (one with _html5 and the other without)
http://lib-php.usc.edu/libraries/about/reference/tutorials/avoiding-plagiarism/story.html
http://lib-php.usc.edu/libraries/about/reference/tutorials/avoiding-plagiarism/story_html5.html
Also please go through http://usclibraries.adobeconnect.com/academicintegrity
Also please go to https://myviterbi.usc.edu/ and watch a video on Academic Integrity Introduction.

Another important resource is the Student Judicial Affairs and Community Standards (SJACS) website .
Please go through the guidelines for academic integrity review process, which can be found in the Student Conduct Code in the current SCampus at https://policy.usc.edu/student/scampus/, Part B, Section 13. Please familiarize yourself with these standards and expectations concerning academic

integrity.
University policy requires that all academic integrity violations are reported to Student Judicial Affairs and Community Standards (SJACS) if the student is an undergraduate and to the VSoE if the student is a graduate student.

We will try to make the assignments due on times far from the class time.
This is to make sure that students do not miss classes to complete their assignments.

Please check your email regularly. Also visit the DEN D2L regularly at https://courses.uscden.net/
D2L stands for Desire2Learn, a Learning Management System used by DEN.
https://gapp.usc.edu/graduate-programs/den/technical-support/Desire2Learn

4. Design/simulation labs sequence:

Example Weights of the labs: Note that some labs have zero weights as you are not asked to submit these labs. However, you are still responsible for reading the lab, understand the design, and are able to answer questions on these items also on the exams. Labs and HWs vary slightly from semester to semester. The list below is from a recent semester.

RTL LABS		
#	Points	weight
1P1	100	0.5
1P2	100	0.7
1P3_M1	100	0.6
1P3_M3	100	0.6
1_Paper	100	0.6
2_Merge_P2	100	0.0
2_Merge_P4	100	1.2
2_Merge_Paper	115	1
FIFO_P1	100	0.6
FIFO_P2	100	0

ALU LABS		
3	100	0.8
3_paper	100	0.6

CPU LABS		
4P1	0	0
4P23	0	0
4P4	100	1.1
6P4	100	1.1
6P5	0	0
7P1	0	0
7P1&P2 Paper	100	1.2
7P3_SP1&2 Paper	100	1.2
7P3_SP1	100	1.2
7P3_SP2	0	0
7P3_SP3	100	1.2
7P3_SP4	100	0
ROB_P1	100	0
ROB_P2	100	1.3

Approximately one lab (or one part of one lab) will be assigned every week starting from the second week.

The labs make up **25%** to **30%** of your course credit.

0) Introduction to Verilog HDL entry and simulation in Modelsim

1) Max. Min. finder State Machine Design Lab #1 Part #1, Part #2, Part #3 (M1, M2, ~~M3, M4~~)

2) Merge Sort lab Lab#2 Part #2 and Part #4

3) Design of a 32-bit ALU Lab #3

4) FIFO and its application

5) Multi-cycle CPU Design Lab #4 Part #4 (only paper submission)

6) Pipeline labs
Design of a 3-element adder Lab #7 Part #1, #2,
Design of a simple pipeline Lab 7 Part #3 (Sub parts SP1, SP2)
RTL Coding of a simple pipeline Lab 7 Part #3 (Sub parts SP3, SP3)

7) Design of a Pipelined CPU Lab #6 Part #4 and Part #5 (only paper submissions)

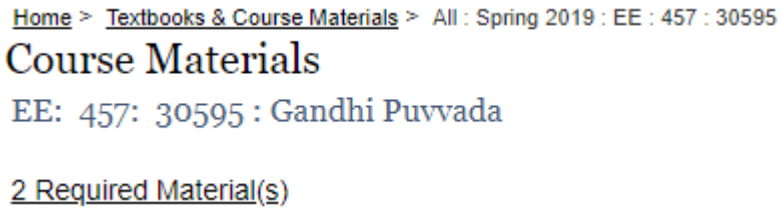
8) ROB and its application

5. Readings:

The required readings are class notes and sections of the textbook. Please make it a practice to read regularly. It is important to clarify any items that are not clear in that week itself. Students, who postpone reading, gradually drift away from the rest of the class and eventually perform very poorly on the exams and design/simulation labs.

Primary References:

Class Notes (required): Please buy from the university (USC) bookstore.
Remote students can place their orders online for the class notes and other items. Links to bookstores:
www.usctext.com
http://www.bkstr.com/usctextstore/shop/textbooks-and-course-materials
If there is any problem, please call (213) 740-TEXT and also let me know if the problem cannot be resolved.



Lab Manual: We prefer to distribute the lab assignments progressively as pdf files. This allows us to review and revise each assignment (if needed) and post it on the D2L.

Textbook/Verilog Guide:
1. Computer Organization & Design - The Hardware and Software Interface 5th edition
By D. A. Patterson (Berkeley) and J. L. Hennessey (Stanford)
We do not use the textbook that much. Some students manage without the textbook. But this is a very good book to buy and keep.
You can buy it from the university (USC) bookstore or any place (such as online bookstores).
http://store.elsevier.com/Computer-Organization-and-Design/David-Patterson/isbn-9780124077263/
If you have the 4th edition, that is fine too.

2. The Verilog 2001 Reference Guide by Esperan (Cadence)
You need this for your Verilog-based design/simulation labs. **You can use it in the EE457 exams**. Esperan (Cadence) does not sell it to individuals. They provided the pdf file to us free. It is posted on the D2L. We will bring a few printed copies to the exam hall and you can borrow a copy for a short time.

Secondary References (Do not buy these):

1. EE101 and EE354L (EE254L) Textbook: Digital Design Principles and Practices By John F. Wakerly
2. EE557 Textbook: Parallel Computer Organization and Design by Dubois, Annavaram, and Stenstrom
3. Computer Architecture - A Quantitative Approach By D. A. Patterson and J. L. Hennessy

6. Course Schedule by week for Spring 2018:

Chapter numbers point to chapters in my class notes (http://www-classes.usc.edu/engr/ee-s/457/EE457_Classnotes/).
Homeworks and labs are due generally 1 week after they are assigned.
Due dates calendar has been posted.

# of lectures	Lecture #	Item	Homework /Lab
2	1, 2 Week #1 1/8-1/10	**Ch#1** Intro to course, review of prerequisite material, Review data path and control unit design, Moore and Mealy, Glitches in control signals, Data registers with Data enable, State diagram design, All Inclusive and Mutually Exclusive rules, Concurrent RTL operations in RTL design.	HW#1
0		Verilog coding: Watch the 6-part EE354L lectures at home and learn by yourselves. Install Modelsim/Questasim and learn to use the tool by yourself	Tools installation and/or VDI
1	3 Week #2 1/15-1/17	Compare and contrast: state diagram vs. flow-chart, Min-Max (a 4-part lab: P1, P2, P3-Method1, P3-Method-3)	Lab #1
1	4 Week #2 1/15-1/17	**Ch#2** Performance, MIPs, MFLOPs	HW #2
2	5, 6, Week #3 1/22-1/24	**Ch#3** MIPs ISA, SLT, SLTU lw, sw, Byte addressable processors, memory addresses. also cover word addresses in a byte addressable processor	HW#1B
1	7 Week #4 1/29	**Ch#4 P1** Review overflow detection in unsigned and signed arithmetic and ALU design	ALU lab Lab #3
2	8, 9 Week #5 1/31, 2/5	**Ch#5 P1** Single Cycle CPU,	HW #5A (Single-cycle CPU)
1	10 (no lecture) Week #5 2/7	**Quiz exam** on Thursday Feb. 7, 2019 5:00 PM-8:00 PM in Room: _____	Quiz slot was TBA

2	11, 12 Week #6 2/12-2/14	**Ch#5 P2** multi-cycle CPU Datapath and control design **Ch#5 P2** Multi-cycle CPU 2nd edition design	Lab 4 Part #4 (Multi-cycle CPU) (paper submission) HW #5B (Multi-cycle CPU)
4	13,14, 15, 16 Week #7,8 2/19-2/28	**Ch#6** 5-stage pipeline: data dependency solutions (Compiler solution, HDU & FU), and branch implementations (late branch vs. early branch), branch delay slots. Also cover exceptions.	Pipelining Lab 6 – Part 4 (paper submission)
2	17, 18 Week #9 3/5-3/7	**Ch#7 P1** Cache: Mapping techniques, CPU address division into fields and connect address to Cache Data RAMs, Cache Tag RAMs,.	Cache HW #6 Pipeline lab #7 P1 and P2 paper
	Week #10 3/12-3/14	**Spring Recess March 10-17**	
1	19 Week #11 3/19-3/21	**Ch#7 P2** Virtual memory: Multi-level page table, PTBR, principle of inclusion. TLBs, and interleaved main memory	FIFO lab
1	20 (no lecture) Week #11 3/19-3/21	**Midterm exam** on Thursday March 21, 2019 5:00 PM-8:00 PM in Room: _____	Quiz slot was TBA
2	21, 22 Week #12 3/26-3/28	Virtual memory, Exceptions, Brach Prediction, 1-bit and 2-bit predictors, BPB, BTB	Virtual Memory HW #7
2	23, 24 Week #13 4/2-4/4	Out of order execution and Tomasulo Part 1 (IoI_OoE_OoC), WAR and WAW hazards in OoO execution, IFQ (Instruction prefetch queue), dispatch unit, issue queues, issue unit, CDB, ROB	Lab #7 P3 Sub Parts 1, 2 (paper submission)
2	25,26 Week #14 4/9-4/11	Tomasulo Part 2 (IoI_OoE_IoC), ROB, ROB search, Speculative execution and selective flushing if branch was mispredicted, exception handling,	ROB lab
2	27, 28 Week #15 4/16-4/18	**Ch#9** Parallel processing, semaphores, Read-Modify-Write (RMW) race, atomic operations on shared variables, CMP, Snoopy Cache Coherency protocols, Write through vs. write-back, MSI, MOESI	Pipeline RTL coding lab Lab #7 P3 Sub Parts 3, 4
1	29 Week #16 4/23-4/25	CMT, Thread-level parallelism, non-blocking cache, MPI	
1	30 Week #16 4/23-4/25	Locks, Atomic operations, LL and SC instructions in MIPs	
		Classes end on Apr. 26, 2019 Friday. Study Days Apr 27-30 USC calendar	
		Final exam on Tuesday, May 7, 2019 either 3:30 PM to 6:30 PM or 4:30 PM - 7:30 PM PST Official slot of 4:30-6:30 PM extended by 1 Hr. Please see the exceptions list at the bottom of https://classes.usc.edu/term-20191/finals/ Electrical Engineering 109, 354, 457 Tuesday, May 7 4:30-6:30	Final exam slot extended by one hour

Statement on Academic Conduct and Support Systems

Academic Conduct:
Plagiarism – presenting someone else's ideas as your own, either verbatim or recast in your own words – is a serious academic offense with serious consequences. Please familiarize yourself with the discussion of plagiarism in *SCampus* in Part B, Section 11, "Behavior Violating University Standards" https://policy.usc.edu/scampus-part-b/. Other forms of academic dishonesty are equally unacceptable. See additional information in *SCampus* and university policies on scientific misconduct, http://policy.usc.edu/scientific-misconduct.

Support Systems:
Student Counseling Services (SCS) - (213) 740-7711 – 24/7 on call
Free and confidential mental health treatment for students, including short-term psychotherapy, group counseling, stress fitness workshops, and crisis intervention. https://engemannshc.usc.edu/counseling/

National Suicide Prevention Lifeline - 1-800-273-8255
Provides free and confidential emotional support to people in suicidal crisis or emotional distress 24 hours a day, 7 days a week. http://www.suicidepreventionlifeline.org

Relationship and Sexual Violence Prevention Services (RSVP) - (213) 740-4900 - 24/7 on call
Free and confidential therapy services, workshops, and training for situations related to gender-based harm.
https://engemannshc.usc.edu/rsvp/

Title IX Preserving the civil rights of the campus community
http://titleix.usc.edu/ http://titleix.usc.edu/prohibited-conduct/ http://titleix.usc.edu/resources/

Office of Equity and Diversity (OED)/Title IX Compliance – (213) 740-5086
Works with faculty, staff, visitors, applicants, and students around issues of protected class. https://equity.usc.edu/

Bias Assessment Response and Support
Incidents of bias, hate crimes and microaggressions need to be reported allowing for appropriate investigation and response. https://studentaffairs.usc.edu/bias-assessment-response-support/

The Office of Disability Services and Programs
Provides certification for students with disabilities and helps arrange relevant accommodations. http://dsp.usc.edu

Student Support and Advocacy – (213) 821-4710
Assists students and families in resolving complex issues adversely affecting their success as a student EX: personal, financial, and academic. https://studentaffairs.usc.edu/ssa/

Diversity at USC
Information on events, programs and training, the Diversity Task Force (including representatives for each school), chronology, participation, and various resources for students. https://diversity.usc.edu/

USC Emergency Information
Provides safety and other updates, including ways in which instruction will be continued if an officially declared emergency makes travel to campus infeasible, http://emergency.usc.edu

USC Department of Public Safety – 213-740-4321 (UPC) and 323-442-1000 (HSC) for 24-hour emergency assistance or to report a crime.
Provides overall safety to USC community. http://dps.usc.edu