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High-performance Pipelined Architecture for Tree-based IP lookup

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Background

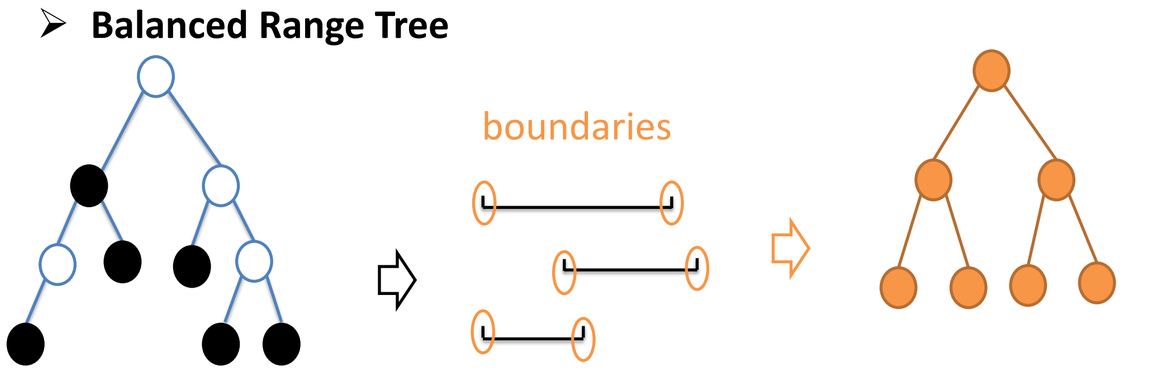
- High-speed Internet
  - 40%~50% bandwidth growth per year
  - 10/40 Gbps → 100/400 Gbps
  - IPv4 → **IPv6**

- IP address lookup
  - Find the **longest prefix match (LPM)** for the input IP in the routing table

Motivation

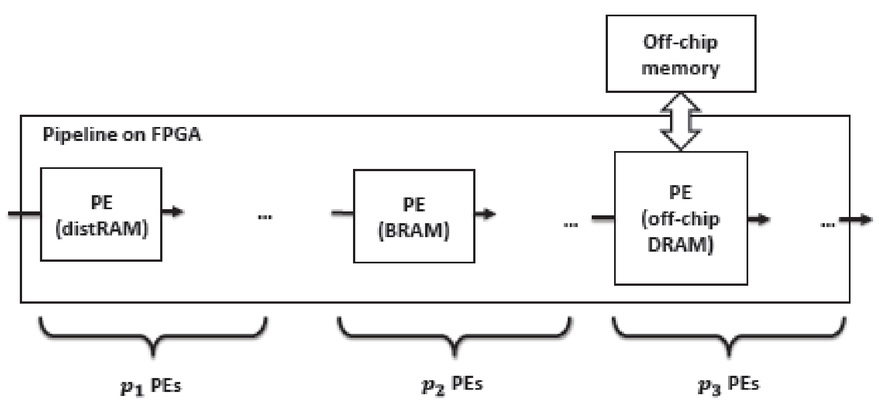
- Hardware-accelerated platforms
  - TCAM
    - Expensive, power-hungry
  - **FPGA**
    - Reconfigurable
    - High-speed I/O interface

- Trie-based approach → too many memory accesses
- Hash-based approach → difficult to scale performance
- Tree-based approach
  - **Balanced Range Tree**



Challenges

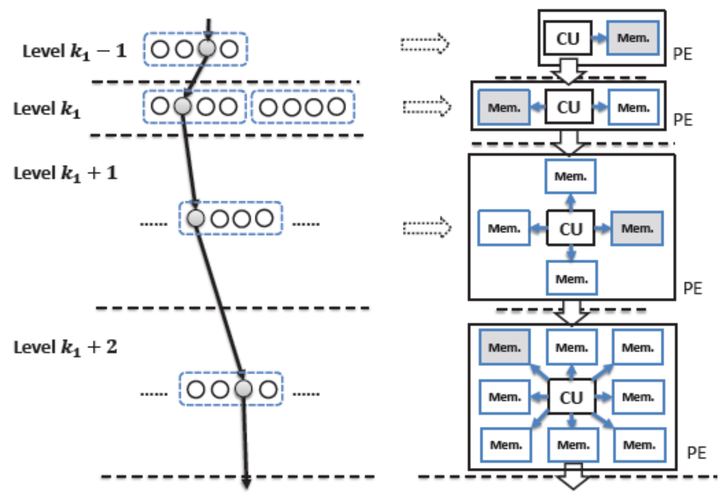
- Efficient hardware support for tree-based IP lookup
  - **Scalability** to support large routing tables



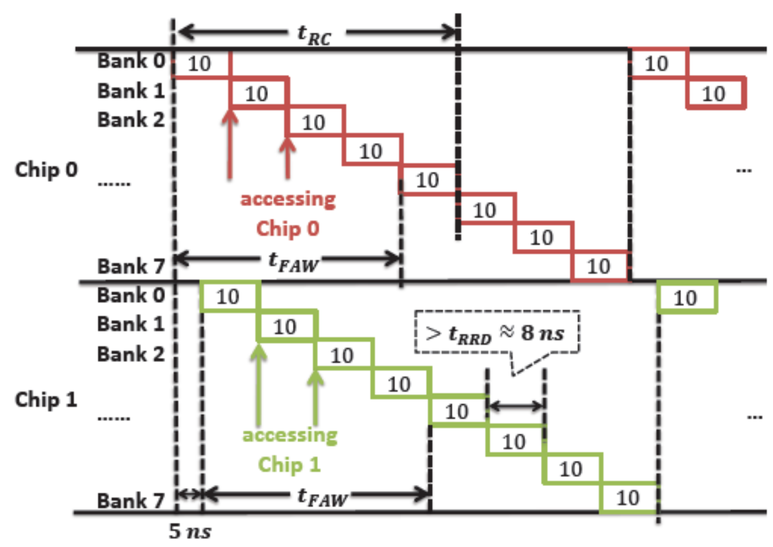
  - **High performance** → novel pipeline architecture

Architecture

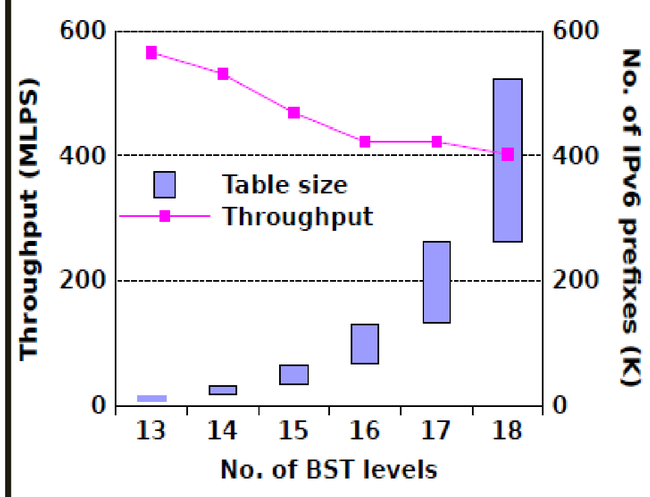
- Distributed RAM stages: **2-dimensional layout**



- BRAM stages: **Split-tree architecture**
- Off-chip memory stages: **Data replication**



Experiments



- 400 MLPS throughput
- 256K -512K IPv6 prefixes
- 59% of logic resources and 19% of total BRAM
- 6.6 × TCAM power efficiency (η)

Solution	Our design	TCAM
Throughput (MLPS)	400	360
Worst-case IPv6 Routing Table Size (K)	256	1024
Power (W)	18.74	-
Delay per Lookup (ns)	282.0	1843.0 [6]
Energy Consumption per Lookup (μJ)	5.28	127.55 [6]
η (nJ/MLPS)	0.052	0.346

Future Work

- Explore efficient mapping from other data structures onto hardware for network applications
- Large-scale IP lookup using hashing mechanism

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