Logic-on-Logic Stacked 3-Dimensional Integrated Circuits

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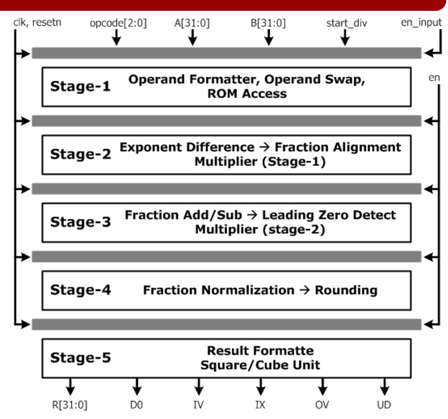
Introduction

- A three-dimensional integrated circuit (3DIC) is a chip in which two or more active layers are integrated both vertically and horizontally into a single circuit
- 3DIC advantages: reduced interconnect length, high device density at small form factor, can stack heterogeneous devices
- Why Logic-on-Logic stacked 3DIC? Improved performance, chip-security, low cost possible, and smaller chip footprint
- Challenges: lack of manufacturing standards, design rules and 3DIC-specific CAD tools, and thermal issues
- Research focuses on building efficient 3DICs using current CAD tools by introducing new techniques where necessary
- A 3DIC floating-point unit (FPU) is implemented to identify the limitations of current tools
- This experiment inspired new design partitioning techniques

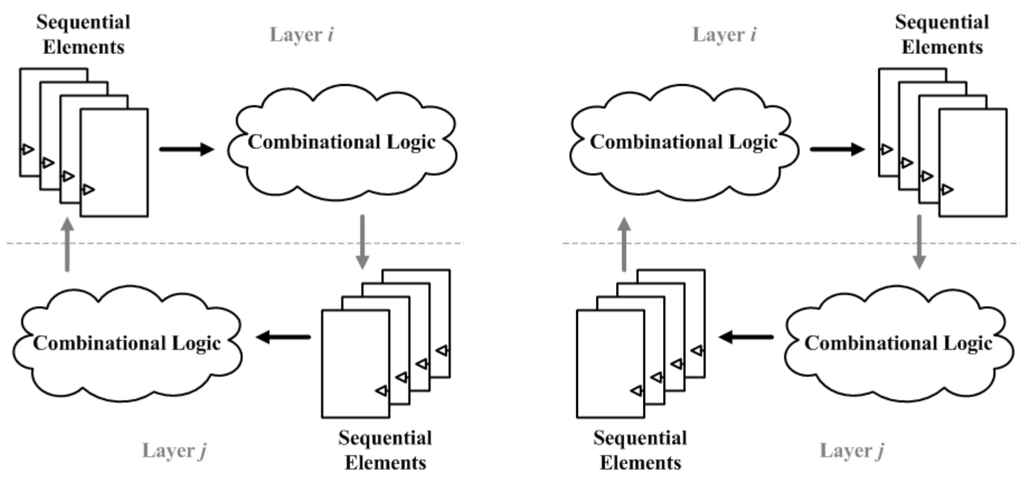
Single-Precision Floating-Point Unit

- 5-stage pipelined architecture
- Single 2-stage pipelined multiplier
- Taylor series expansion based division with squaring and cubing units
- Non-linear pipeline division operation
- Latency can be 5, 8, or 12 cycles



Design Partitioning Techniques

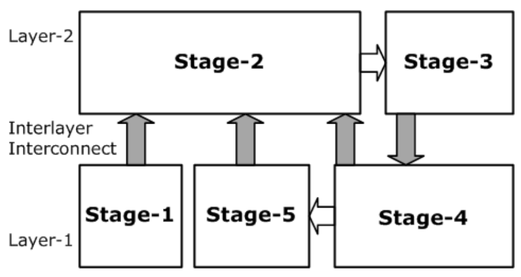
- Combinational to Sequential (C2S): Each signal traversing a vertical interconnect is an output of combinational logic driving the data-input of a sequential element in the neighboring layer
- Sequential to Combinational (S2C): Q-outputs of the flip-flops of a layer tunnel through layers and drive combinational logic in the adjacent layers



- Hybrid: Partition only at input or output of sequential nets
- Proposed techniques are independent of targeted number of layers and design size
- Search space for partitioning is significantly reduced
- Simpler logical effort optimization problem when compared to partitioning between combinational logic
- Allows a pipelined functional-unit block to be split across layers, without any need for redesigning the unit
- These techniques simplify manual design partitioning

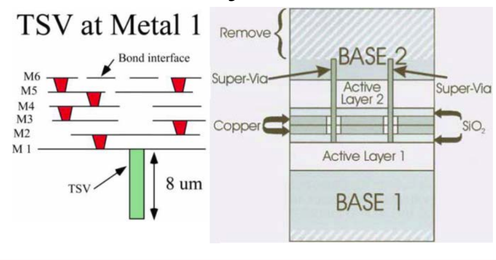
3D FPU

- Design has two layers, because of
  - Small size of FPU design
  - Two-tier constraint by MOSIS
- Manually partitioned into two layers
- Two variants are designed
  - C2S and S2C partitioning
- This design enables the use of current tools and cell libraries



3DIC Technology

- MOSIS 3DIC package uses Tezzaron-Global foundries two-layer 130nm fabrication technology
- M6 metal layer micro-bumps interconnect the layers
- Layers are face-to-face bonded
- I/O and power signals use TSVs called Super-Vias
- Top-tier with pads is thinned



3DIC Design Flow

Design Partitioning: Manually partitioned at functional unit level, into two layers.

Synthesis: Each layer is synthesized independently. Faster layer is synthesized with slower layer's clock to reduce area.

Timing Analysis: Timing is analyzed on a top level module that instantiates the post-synthesis modules of the two layers.

Negative Slack? — YES → High delay on inter-layer signals? — YES → Modify output load constraints → Synthesis

Negative Slack? — NO → Ready for post-synthesis design flow

High delay on inter-layer signals? — NO → Increase target clock period → Synthesis

Place and Route Step-1: Layer-1 is placed and routed using 3DIC process design rules. The inter-layer signals are assigned to bumps using a greedy instance-based approach.

Place and Route Step-2: Layer-2 is placed and routed using a mirrored version of signals to bumps assignment of the first layer as a reference.

Clock Tree Synthesis: CTS is executed independently on each layer. The clock insertion delays are balanced to force the clock signal to reach both layers at the same time.

Final Verification: Timing is verified. Followed by logic equivalence check and SDF back-annotated simulation, to validate the logical correctness of the 3DIC.

Results and Conclusions

	S2C 3D FPU	C2S 3D FPU	2D FPU
Clock Period	6.37ns	6.61ns	6.83ns
Footprint	306x306 um^2	306x306 um^2	400x400um^2

	S2C 3D FPU		C2S 3D FPU	
	Layer-1	Layer-2	Layer-1	Layer-2
Avg. Wire Length (um)	1.08e+1	1.22e+1	1.25e+1	9.70e+0
Power (mW)	4.586	6.256	4.639	6.08
Cell Area (um^2)	81463	73972	62736	79590

- Based on 3DIC implementation experiment using current tools:
  - Proper design partitioning technique is required for use of current tools
  - Automated partitioning and simultaneous synthesis of all layers are required
  - Current tools are adequate for timing verification
- Proposed partitioning techniques when integrated into tools can speed up tools performance and are more likely to achieve near-optimal solution
- Results show that the two variants of 3D FPU are 41.5% smaller in foot-print and up-to 7% faster compared to 2D FPU

Related Publications

Gopi Neela and Jeffrey Draper. *Logic-on-Logic Partitioning Techniques for 3-Dimensional Integrated Circuits*. IEEE International Symposium on Circuits and Systems (ISCAS), May 2013.

Gopi Neela and Jeffrey Draper. *Challenges in 3DIC implementation of a design using current CAD tools*. IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), August 2012.