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High-performance Dynamically Updatable Packet Classification

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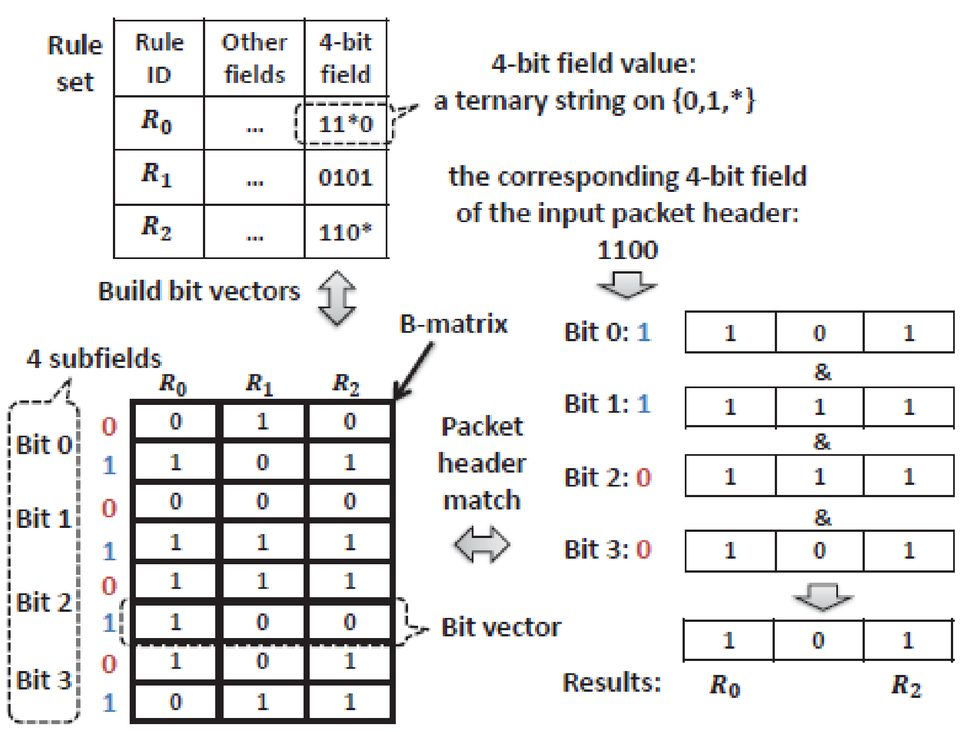
Background

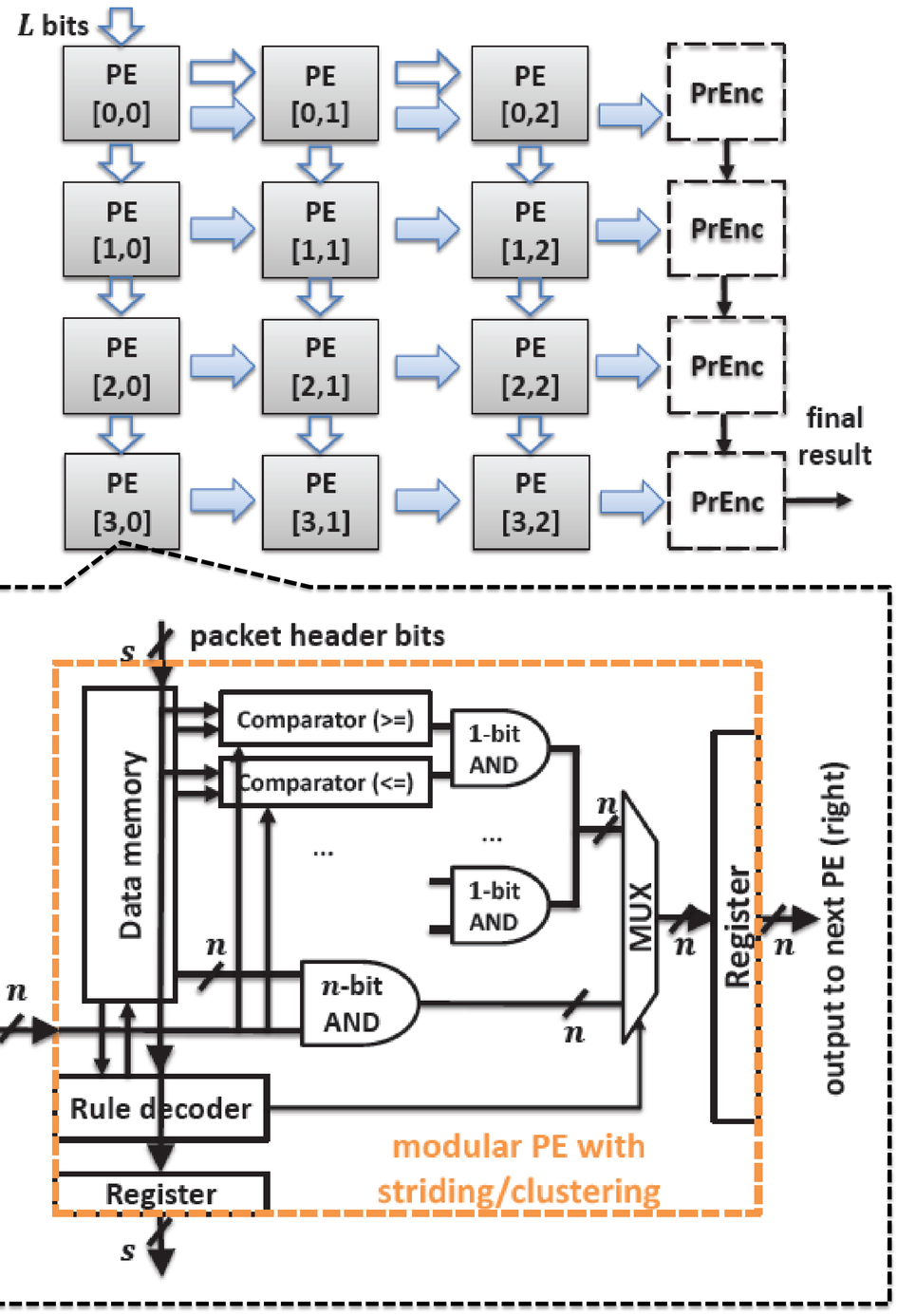
- **Network traffic**
  - 40%~50% bandwidth growth per year
  - Network security: worms, virus, etc.
- **Packet classification**
  - Classify packets during runtime
  - Kernel function of routers

Motivation

- **FPGA platform**
  - Reconfigurable, flexible
  - Massive on-chip bandwidth
- **Focus on performance**
  - Main performance metrics: **scalability, throughput, update rate**
- **Prior Bit Vector (BV) based approaches**
  - Map each bit of the rule into memory
  - No support for dynamic updates



Architecture & Update Algorithms



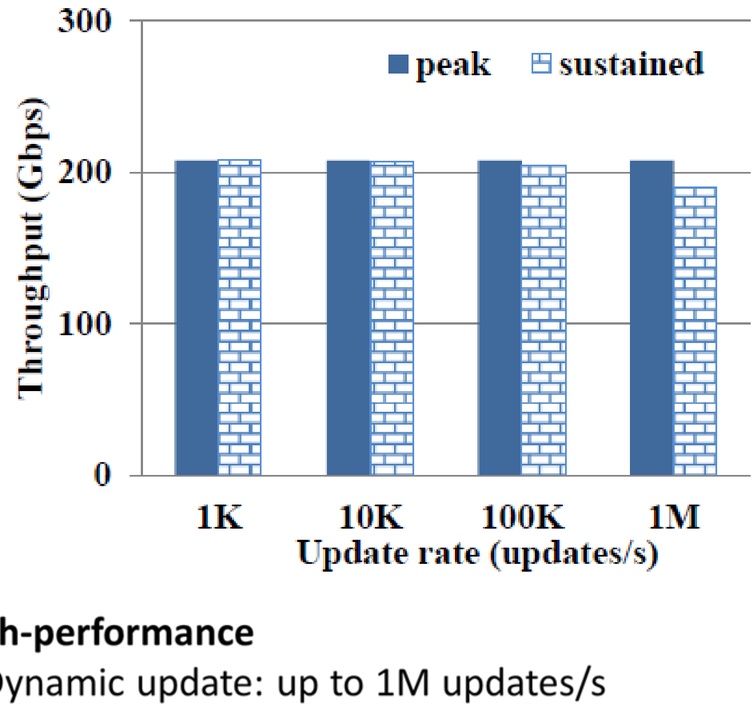
- **Modification**
  - Modify: Construct new bit vectors, replace the old ones
- **Deletion**
  - Keep a "valid" bit for each rule, set the "valid" bit to "0"
- **Insertion**
  - Reuse the location whose valid bit is "0"
  - Construct the BV, modify the invalid rule

Challenges

- **Performance**
  - Limited resources
  - A large number of classification rules
  - High throughput requirement
- **Dynamic updates**
  - Modify/delete/insert a rule
  - Impact on throughput
  - e.g. delete R_1 from the rule set below

RID	SIP	DIP	SP	DP	Protocol	Priority	Action
R_0	95.105.143.51/32	204.13.218.182/32	0-65535	0-65535	0x01	1	Action 0
R_1	95.105.143.51/32	39.240.26.229/32	0-65535	1521-1521	0x06	2	Action 2
R_2	152.175.65.32/28	248.116.141.0/28	24032-24032	123-123	0x11	1	Action 1

Experimental Results



- **High-performance**
  - Dynamic update: up to 1M updates/s
  - Throughput: 200Gbps throughput for 1K rules
  - 4× TCAM power efficiency

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