400G+ Single Chip Packet Classification

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Goal: High-speed, Low Power and Secure Packet Forwarding in the Internet

High-speed networking
- 10 Gbps (OC192) → 40 Gbps (OC768)
- 100/400 Gbps and Terabit networks

Network security
- Prevents attacks, unauthorized access, etc.,
- Software/hardware firewalls

Green Internet
- Reduce power consumption in the network
- Brute force TCAM → Algorithmic CAMs

Multi-field packet classification
- Most prominent: 5-field
- Inspect <SIP, DIP, SP, DP, PRT>
- Lookup a classifier to identify forwarding info.
- Block or filter network traffic

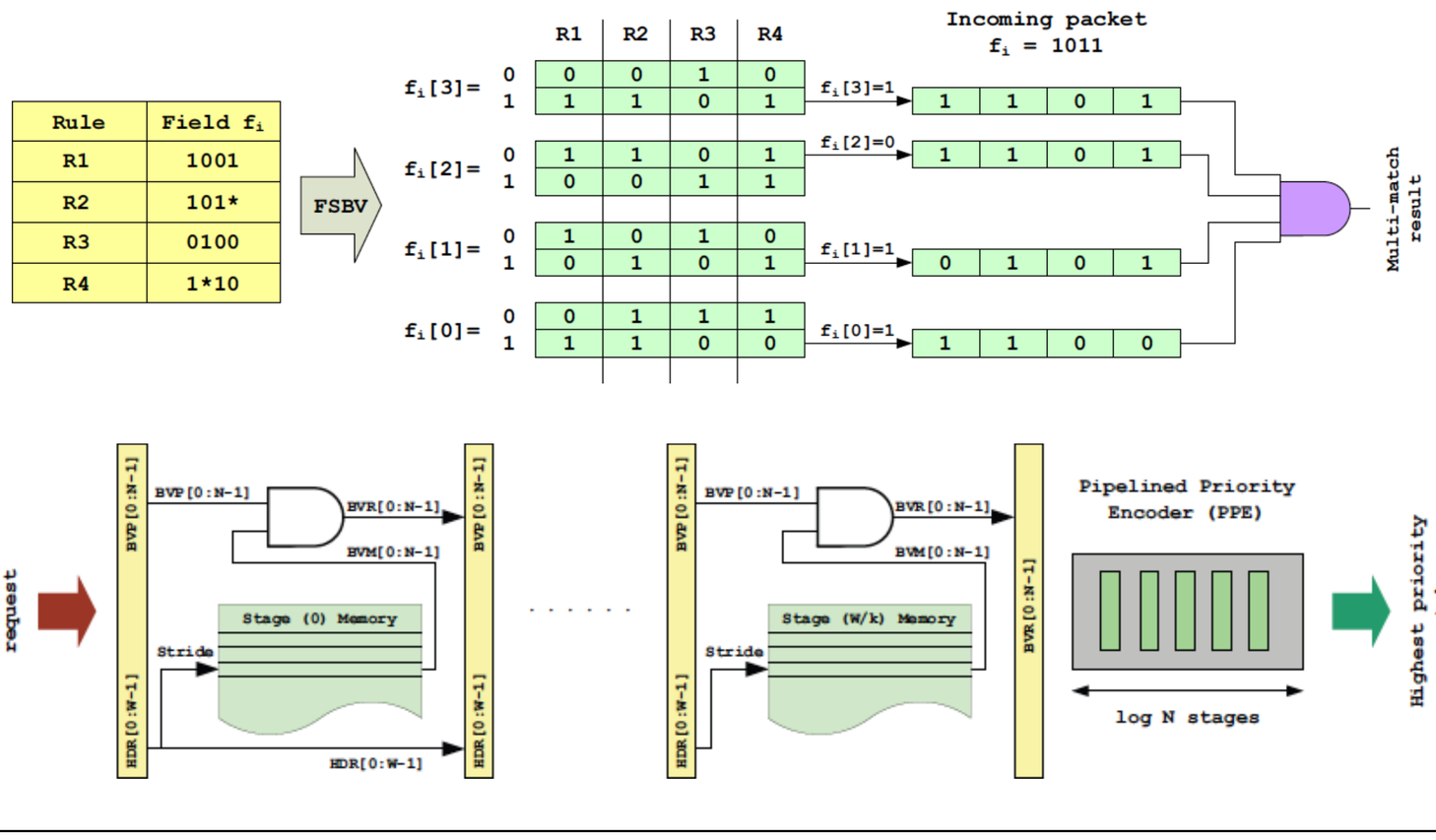
Field Programmable Gate Array (FPGA)
- Abundant parallelism, reconfigurability, pipelining
- Xilinx Virtex-6 VLX760
  - 758K Logic cells
  - 8Mb distributed RAM
  - 26Mb block RAM

Approach

Field-Split Bit-Vector (FSBV)
- Rule of length W → W sub-fields
- Each sub-field → N-bit bit-vector
- N – # rules in classifier

StrideBV
- Consider a stride k of the rule
- W/k sub-fields
- Simple architecture: Single N-bit AND operation per pipeline stage
- Independent of classifier features
- Flexibility in adjusting
  - Packet latency
  - Memory usage
  - Power consumption

StrideBV Architecture



Design Considerations

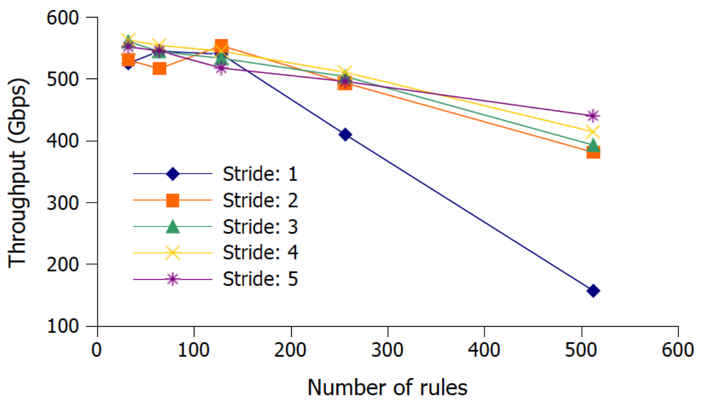
FPGA architecture
- Stage memory
  - Distributed RAM over block RAM → High-speed
  - Dual-ported SRAM based pipeline
- Multi-pipeline parallel architecture
  - Improve throughput
  - 1x400G or 4x100G configuration
- Multi-stage priority encoder
  - Report highest priority match

Classifiers
- Bro/Snort Intrusion Detection Systems (IDSs)
- Real-life firewall classifier sizes: 50~1K rules

Summary

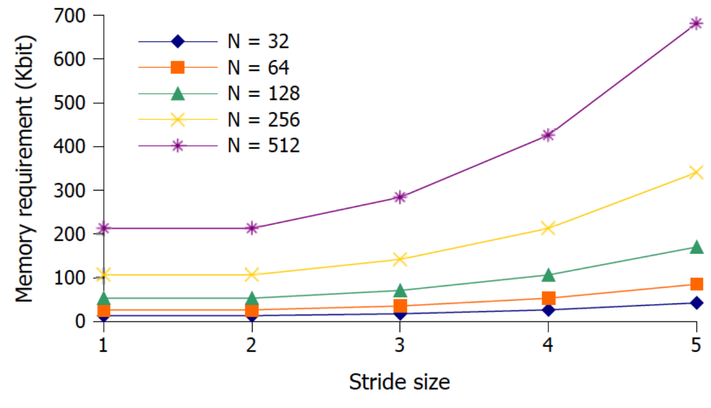
- The first single chip solution for 400Gbps packet classification
- Performance independent of classifier features
- 2.5x power efficiency compared with state-of-the-art

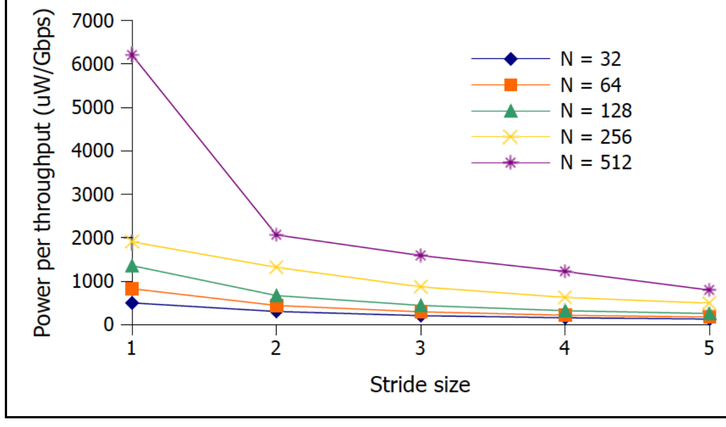
Performance



Throughput gradually decreases with classifier size due to the increase in FPGA signal routing

Memory requirement increment proportional to: $\frac{2^k}{k}$





With increasing stride size, power efficiency increases.

When memory power starts dominating, power efficiency degrades

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